A Sub-Nanosecond Resonant-Type Monolithic T/R Switch for Millimeter-Wave Systems Applications

Mohammad Madihian, Laurent Desclos, Kenichi Maruhashi, Kazuhiko Onda, and Masaaki Kuzuhara

***Abstract*—This paper is concerned with the design consideration, fabrication process, and performance of a V-band monolithic transmit/receive (T/R) switch for millimeter-wave wireless networks applications. The developed switch integrated circuit (IC) has a novel structure in which to pass a signal, it presents a parallel resonant circuit to the signal by forward biasing a pair of switching heterojunction FET's (HJFET's), but to block the signal, it presents a series resonant circuit to the signal by reverse biasing the switching HJFET's. With a control voltage of 0/3.2 V, the developed T/R switch exhibits a minimum insertion loss of 3.9 dB, a maximum isolation of 41 dB, and a high switching speed of 250 ps, over 57–61 GHz. The monolithic T/R switch chip size is 3.3 mm × 1.7 mm.**

I. Introduction

Development of high-speed transceiver transmit/receive (T/R) switches with excellent isolation characteristics are indispensable for 100–200-Mb/s millimeter-wave indoor local area networks (LAN's) and automotive-sensors applications [1], [2]. FET switches are advantageous over their p-i-n diode counterparts for their fast switching speed, RF-isolated bias port, negligible power dissipation, and monolithic realizability [3]–[5].

A conventional FET T/R switch is constructed by essentially incorporating a series/shunt pair of FET's between the antenna and receiver (RX) ports, as well as between the antenna and transmitter (TX) ports [6]–[8]. Such a structure, which has been applied to frequencies below 20 GHz, exhibits an appreciable isolation characteristics, however, has a relatively low switching speed of several nanoseconds. To improve the speed characteristics of the switch while keeping the isolation high, the series FET's in the above structure have been replaced by transmission lines having specific length and characteristics impedance [5], and switching speeds of 0.5 ns at 18 GHz and 1 ns at 60 GHz have been recently reported [9], [10].

The FET T/R switches reported so far block a signal when a control voltage applied to the gate terminal of the shunt FET is 0 V, but pass the signal when the control voltage is equal to or lower than the shunt FET's pinchoff voltage. To cancel out a mismatching effect of the FET drain–source pinchoff capacitance on the insertion characteristics, it is required to incorporate a parallel-resonating inductance between the drain terminal and the ground, which in turn, dc grounds the drain terminal, and thus, deteriorates low-frequency insertion characteristics of the switch.

Utilizing a series/parallel resonance concept, this paper describes an FET T/R switch featuring a simple structure suitable for sub-nanosecond class millimeter-wave transceiver applications. Circuit design, fabrication process, and experimental results for the case of a coplanar waveguide (CPW) V-band T/R switch using 0.15 μm× 300 μm AlGaAs/InGaAs heterojunction FET's (HJFET's) are presented.

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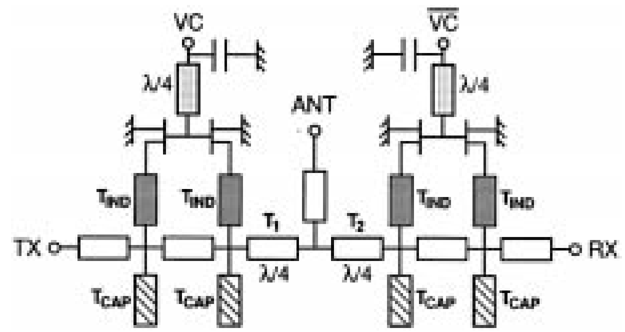

Fig. 1. V-band T/R switch schematic circuit diagram.

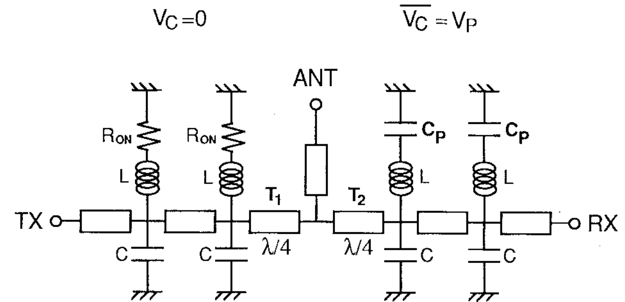

Fig. 2. Switch equivalent circuit for the case of $V_C = 0$ and $\overline{V_C} = V_P$.

II. Circuit Design

A schematic circuit diagram for the CPW V-band FET T/R switch is shown in Fig. 1. The switch consists of TX and RX arms, each comprising a pair of depletion-type shunt FET's, inductive transmission lines $T_{\rm IND}$ connected in series with each FET and capacitive transmission lines $T_{\rm CAP}$, which are in parallel connection with each $T_{\rm IND}$.

Signal-line segments in the transmitter-to-antenna path, as well as in the antenna-to-receiver path, have a characteristics impedance of 50 Ω. Quarter-wavelength line segments T_1 and T_2 in the transmitter-to-antenna and antenna-to-receiver paths, respectively, provide a high transmitter-to-receiver isolation, to be explained later.

Switch operation is performed by changing control voltages V_C and $\overline{V_C}$ complementarily, which causes an FET pair to be either in an "ON" state or "OFF" state. Quarter-wavelength transmission lines incorporated between the FET gates and the bias port and bypass capacitors are used in each arm to eliminate an RF signal leakage into the FET gate bias circuit.

To explain the operation principles for the present switch, an equivalent circuit for the case of $V_C = 0$ and $\overline{V_C} = V_P$ (FET pinchoff voltage) is shown in Fig. 2, where the drain–source impedance of each FET in the TX arm is represented by the FET "ON" resistance $R_{\rm ON}$, and that of each FET in the RX arm is represented by the drain–source pinchoff capacitance C_P. L and C, on the other hand, are the equivalent inductance and capacitance of $T_{\rm IND}$ and $T_{\rm CAP}$, respectively.

Under such a circumstance, for this structure, in contrast to previously reported switches, by causing an FET pair to be in the "ON" state, the resultant parallel resonant circuit in the corresponding arm (TX arm, for this case) will become "open" and the signal can be transmitted, but on the other hand, by causing an FET pair to be in the "OFF" state, the resultant series resonant circuit in the corresponding

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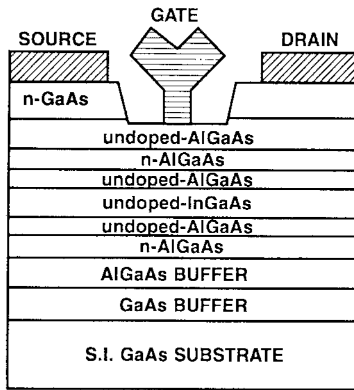

Fig. 3. Cross-sectional view for the AlGaAs/InGaAs HJFET used in the switch chip.

arm (RX arm, for this case) will become "short" and the signal will be blocked. Moreover, the role of quarter-wavelength line segments T_1 and T_2 is to cancel out the effect of a series resonant short circuit in one arm on a signal being transmitted in the other arm, and also to sustain a high transmitter-to-receiver isolation.

The switch was designed for operation at a center frequency of 60 GHz. Based on capacitance measurement results for a discrete 0.15 μm $\times$ 300 μm AlGaAs/InGaAs HJFET, the switch circuit (shown in Fig. 1) was analyzed on a nonlinear circuit simulator to optimize capacitive transmission lines $T_{\rm CAP}$, as well as inductive transmission lines $T_{\rm IND}$, for best port matching, minimum insertion loss, and maximum isolation.

III. Fabrication Process and Device Characteristics

The V-band T/R switch integrated circuit (IC) was fabricated on a 3-in undoped SI GaAs substrate. A cross-sectional view of a molecular beam epitaxy (MBE) AlGaAs/InGaAs HJFET used in the MMIC is shown in Fig. 3. The epitaxial layer structure consists of an AlGaAs/GaAs superlattice followed by GaAs and AlGaAs buffers, a 13-nm $In_{0.2}Ga_{0.8}As$ channel sandwiched between Si-doped $Al_{0.2}Ga_{0.8}As$ layers and an 80-nm n^+-GaAs cap layer. In the FET fabrication process, mesa-isolation, conventional photolithography, electron beam evaporation, and liftoff techniques have been employed. A CPW structure was used for transmission lines, which permits chip size reduction and the possibility of realizing transmission lines with different characteristics impedances without affecting the overall chip layout. To suppress odd modes, metal bridges were extensively employed to connect ground planes along the lines, particularly in the vicinity of a line discontinuity. A metal–insulator–metal (MIM) structure was applied for fabricating dc blocking and bypass capacitors. Details of the fabrication process have been reported elsewhere [11], [12]. The HJFET's used in the switch IC have a gate length of 0.15 μm and a total gatewidth of 300 μm (75 μm$\times$ 4 fingers). Typical transconductance of 380 mS/mm and f_T of 70 GHz, both at a drain bias of 4 V, and a reverse gate–drain breakdown voltage of 10 V have been measured for the HJFET's. Measured pinchoff voltage and corresponding drain-to-source pinchoff capacitance for the HJFET's are -3.2 V and 0.1 pF, respectively. The inductance L and capacitance C were realized, respectively, using 12 μm$\times$ 80 μm and 54 μm$\times$ 1200 μm transmission-line segments.

IV. Performance

Fig. 4 shows the chip photograph for the developed V-band switch. Chip size is 3.3 mm $\times$ 1.7 mm. Cascade Microtech probe station

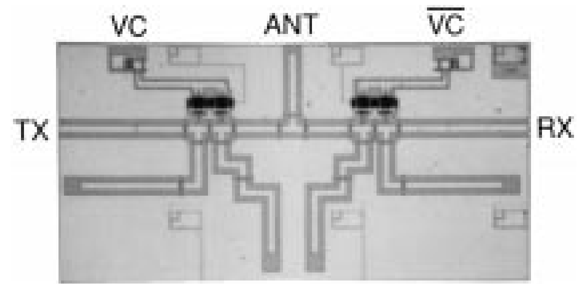

Fig. 4. V-band CPW FET T/R switch MMIC with a chip size of 3.3 mm$\times$ 1.7 mm.

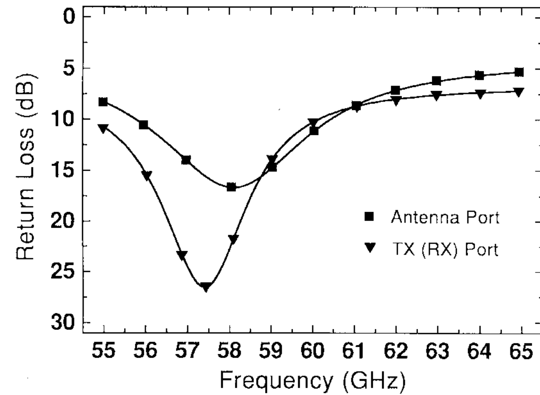

Fig. 5. Small-signal matching characteristics for the antenna and TX (or RX) ports.

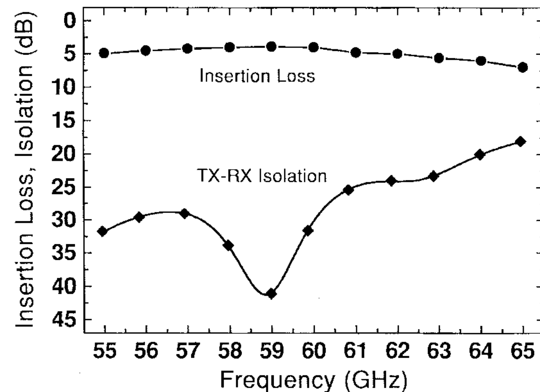

Fig. 6. Measured insertion loss and TX-to-RX isolation characteristics for the switch.

was utilized for on-wafer chip performance evaluation. Small-signal matching characteristics for the antenna and TX, as well as RX ports are depicted in Fig. 5. With respect to Fig. 5, the antenna port exhibits a return loss higher than 10 dB over 56–60.5 GHz. On the other hand, return loss for the TX port during the transmission mode, i.e., $V_C = 0$ and $\overline{V_C} = -3.2$ V is higher than 10 dB over 55–60.5 GHz. This curve also represents the return-loss characteristics for the RX port during the reception mode, i.e., $V_C = -3.2$ V and $\overline{V_C} = 0$. Insertion-loss characteristics during transmission/reception mode and TX-to-RX isolation performance for the switch are shown in Fig. 6. The insertion loss has a minimum value of 3.9 dB at 59 GHz, and remains lower than 5 dB over 56–62 GHz. On the other hand, the TX-to-RX isolation has a maximum value of 41 dB at 59 GHz, and remains higher than 28 dB over 56–61 GHz.

Speed performance for the T/R switch was investigated using a 250-MHz 50% duty pulse with a 0-V/3.2-V level and a rise/fall time

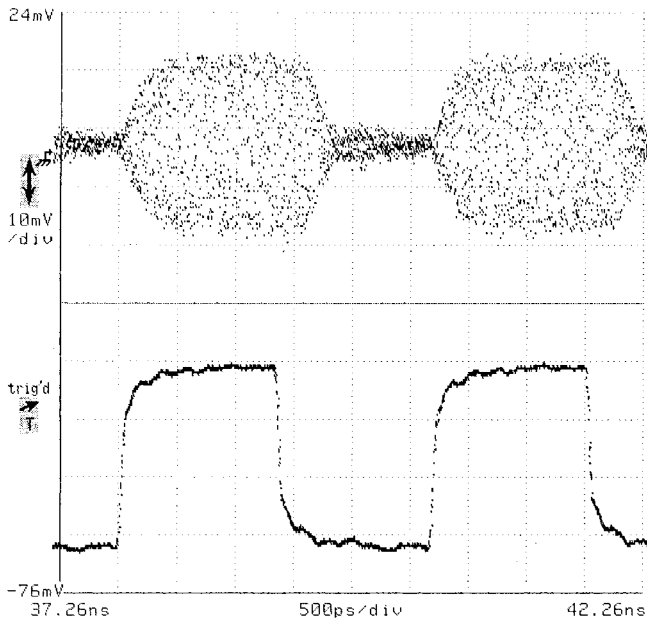

Fig. 7. Switch's speed performance measured using a 250-MHz 50% duty pulse.

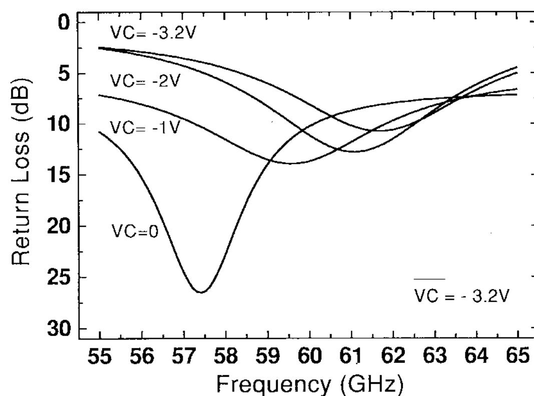

Fig. 8. Control voltage dependence of TX port matching for a fixed $\overline{V_C} = -3.2$ V, and V_C as a parameter.

of 100 ps. As depicted in Fig. 7, the chip exhibited a rise and fall time of 250 ps for a 60-GHz input signal. We believe that the developed monolithic microwave integrated circuit (MMIC) represents the state-of-the-art switching speed among all other circuits reported so far.

A. Effects of Control Voltage Adjustment on Switching Behavior

As was stated earlier, this switch operates based on a series/parallel resonance concept. For a fixed inductance L, the resonant frequency of the switch can be changed by adjusting the control voltages V_C and $\overline{V_C}$ which, in turn, changes the corresponding FET's drain–source capacitance. Recalling Fig. 1, we investigated the effects of V_C change on the TX port-matching and insertion-loss characteristics for a fixed $\overline{V_C} = -3.2$ V. Results, for the cases of $V_C = 0, -1, -2,$ and -3.2 V are summarized in Figs. 8 and 9. With respect to Figs. 8 and 9, while the best port matching and lowest insertion loss have been achieved for a $V_C = 0$, reduction of V_C reduces the return loss and, consequently, increases the insertion loss, until V_C approaches pinchoff voltage (-3.2 V) for which the TX port becomes isolated from the antenna port. Moreover, it can be observed that by reducing V_C, the resonant frequency of the switch, and thus, the operation center frequency of the switch, can be shifted up until V_C approaches -3.2 V, beyond which there will be no significant change.

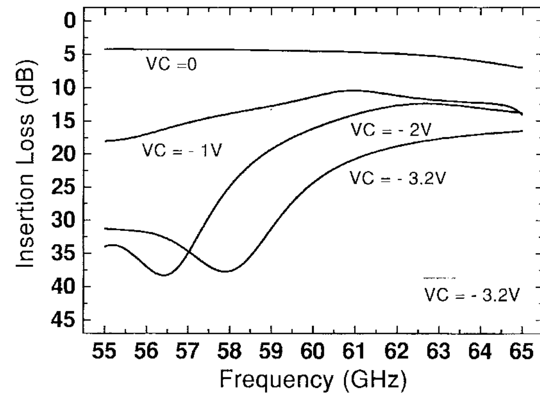

Fig. 9. Control voltage dependence of insertion loss for a fixed $\overline{V_C} = -3.2$ V, and V_C as a parameter.

V. Conclusions

Design consideration and performance for a V-band monolithic T/R switch were described. The developed switch IC has a novel structure in which to pass a signal; it presents a parallel resonant circuit to the signal by forward biasing a pair of switching HJFET's, but to block the signal, it presents a series resonant circuit to the signal by reverse biasing the switching HJFET's. With a control voltage of 0/-3.2 V, the developed T/R switch exhibits a minimum insertion loss of 3.9 dB and a maximum isolation of 41 dB over 57–61 GHz. On the other hand, measured switching speed for the developed chip is 250 ps, which is believed to be the fastest value achieved so far. The monolithic T/R switch chip size is 3.3 mm × 1.7 mm, and the hope is to find applications in high-speed millimeter-wave indoor wireless LAN and automotive-sensors systems.

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Reflection-Type Low-Phase-Shift Attenuator

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***Abstract*— A transmission-type phase-shift attenuator has a poor reflection characteristic at an output port. In this paper, to avoid such disadvantages, a reflection-type low-phase-shift attenuator has been designed and measured. As a result, at a center frequency (1855 MHz), the reflection-type low-phase-shift attenuator has an attenuation of 30 dB, within the limit of 3° phase shift and less than −17-dB reflection characteristics at both input and output ports. It also demonstrates that the performance of the reflection-type low-phase-shift attenuator is better than the transmission-type phase-shift attenuator with the same measurement specifications.**

***Index Terms*—Attenuator, p-i-n diode, reflection type.**

I. Introduction

The circuits generally used in the transmitter of the base station of a modern mobile-communication system consist of high-power amplifiers, linearizers, and so on. The variable attenuator is especially one of the most important control circuit blocks composing linealizers, as well as automatic gain control (AGC) systems. Generally, the attenuators are implemented by using a p-i-n diode or GaAs MESFET with electrically controllable resistance [1] and, in this paper, p-i-n diodes are applied.

A radio-frequency (RF) signal is composed of both magnitude and phase elements, but the phase characteristics can be distorted with the variance of attenuation due to the following structural problem.

In Fig. 1, the S-parameters of the series impedance Z are given by [2]

$$[S] = \begin{bmatrix} \dfrac{Z}{Z+2Z_0} & \dfrac{2Z_0}{Z+2Z_0} \\ \dfrac{2Z_0}{Z+2Z_0} & \dfrac{Z}{Z+2Z_0} \end{bmatrix}. \tag{1}$$

The attenuation constant α can then be written as

$$\begin{aligned} \alpha &= 20 \log \left| \frac{1}{S_{21}} \right| = 20 \log \left| 1 + \frac{R+jX}{2Z_o} \right| \\ &= 10 \log \left[\left(1 + \frac{R}{2Z_o} \right)^2 + \left(\frac{X}{2Z_o} \right)^2 \right]. \end{aligned} \tag{2}$$

In the general case of attenuators, the phase characteristic of S_{21} is

$$\begin{aligned} S_{21} &= |S_{21}| e^{\varphi} \\ &= \frac{2Z_o}{(Z+2Z_o)} \end{aligned} \tag{3}$$

$$\rightarrow \varphi = \tan^{-1} \frac{-X}{R+2Z_o}. \tag{4}$$

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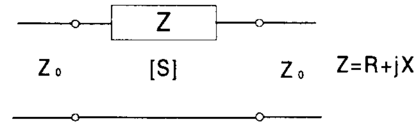

Fig. 1. The equivalent circuit of attenuator.

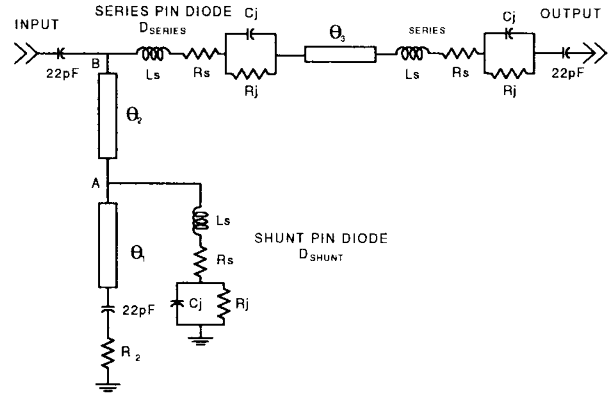

Fig. 2. Transmission-type low-phase-shift attenuator.

As we can observe in (4), the phase characteristic is variable with the variance of attenuation because φ is a function of R. To solve this kind of structural problem, Walker [3] invented the transmission-type attenuator using p-i-n diodes.

Fig. 2 shows the modified Walker version. It was invented in order to enlarge the attenuation by using series connected diodes.

In this circuit, series-connected p-i-n diodes operate as attenuators, while a shunt-connected diode operates as a phase-shift compensation circuit. The characteristic of intrinsic layer resistance of a p-i-n diode is given by [1]

$$R = \frac{W^2}{(2\mu_{ap}\tau I_0)} \tag{5}$$

where

- W width of i layer;
- μ_{ap} ambipolar mobility;
- τ carrier lifetime;
- I_0 dc bias current.

By forward biasing the diodes in Fig. 2, I_o is increased and R_j is near 0 Ω, as can be observed in (5). At this time, the attenuation is minimum and the R_j of the shunt-connected p-i-n diode goes to zero. Thus, point A turns out to be a short and the shunt-connected stub at point B will be sensed as the short stub with electrical length θ_2. For this reason, there is no attenuation caused by R_2.

Alternatively, if I_o is decreased by reverse biasing, then R_j is increased. Thus, the shunt-connected stub at point B has an effect on the entire circuits.

Let the phase of the total system be $\varphi_{R_j=0}$ at $R_j = 0$, and $\varphi_{R_j=\max}$ at $R_j = \max$. If it is possible that $\varphi_{R_j=0} = \varphi_{R_j=\max}$ with controlling θ_1, θ_2, θ_3, and R_j, then no phase shift occurs with the variance of attenuation.

The parameter values of $R_2 = 15$ Ω, $\theta_1 = 15°$, $\theta_2 = 16.46°$, and $\theta_3 = 14.28°$ are applied in experiments.

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